

ECE 300 Projects

1- Layout Aware Test Pattern Generation for Transition Delay Faults

Transition delay fault test patterns generate switching activity in the circuit higher than that of normal mode. In this project, the patterns for transition delay faults are first generated using deterministic ATPG with no random-fill. After the patterns are generated, they must be analyzed to see where in the design (and related power grid) the transitions are happening. This should be used as a metric for compacting the patterns. If there are two patterns that generate a large number of transitions in a local area, then those two patterns should not be merged. If the patterns are generating a large number of simultaneous switching but in different locations in the circuit (i.e. drawing currents from different grids) then those patterns are merge-able. This method helps avoid hot spots in the circuit when applying test patterns.

2- Hard-to-detect Inclusions:

Security and trust have become major concerns for semiconductor companies and agencies. Currently due to lower manufacturing costs, a large number of fabless companies are shipping their designs to low cost foundries overseas. The concern is how we ensure the manufactures design will work as intended.

Hard-to-detect inclusion is considered as one potential attack. A defect, logic element or a small Trojan can be inserted in such areas in the chip and they can go undetected since our ATPG tools cannot provide 100% fault coverage. This should be examined for both stuck-at and transition delay faults. First generate the patterns and if the fault coverage is not 100%, identify the location of such faults and insert a defect. Try to activate the defect in mission mode and show that the chip passed the test but failed in the field. I call this time bomb.

3- Pattern Delay Analysis:

Develop a tool to perform a pattern delay analysis and identify all the paths being affected by each pattern.

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